Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OFFSET NULL**
2. **INPUT -**
3. **INPUT +**
4. **VEE**
5. **OFFSET NULL**
6. **OUTPUT**
7. **VCC**

**.064”**

**1**

**2**

**3**

**4 5**

**7**

**6**

**MASK**

**REF**

**.059”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” x .004” min.**

**Backside Potential: FLOATING**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .059” X .064” DATE: 5/9/22**

**MFG: MOTOROLA THICKNESS .013” P/N: MC1556**

**DG 10.1.2**

#### Rev B, 7/19/02